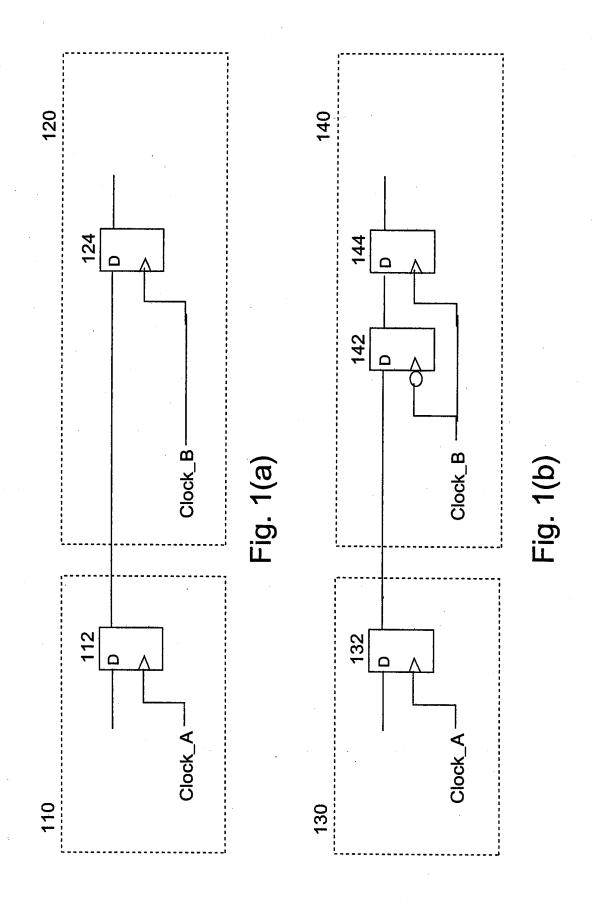
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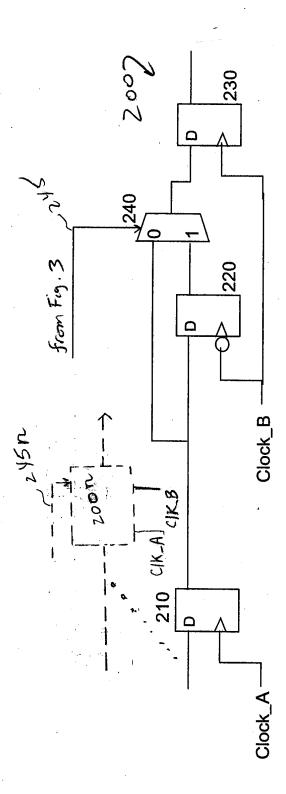


Fig. 2 (Data Path Circuit)

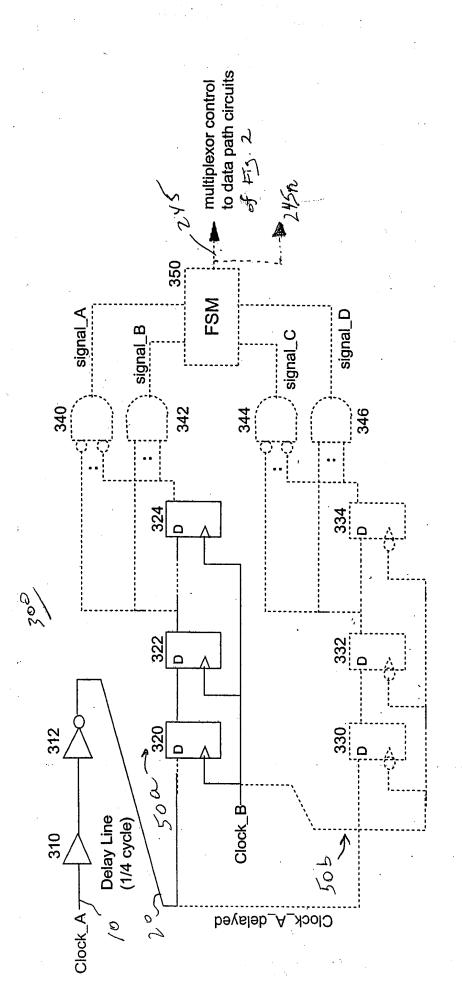


Fig. 3 (Control Circuit)

